UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,615	03/30/2005	Marc Fahlenkamp	1890-0215	1615

50255 7590 03/01/2007

MAGINOT, MOOR & BECK
111 MONUMENT CIRCLE, SUITE 3000
BANK ONE CENTER/TOWER
INDIANAPOLIS, IN 46204

EXAMINER	
HANSEN, STUART ALAN	
ART UNIT	**PAPER NUMBER**
2809	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/529,615	FAHLENKAMP ET AL.	
	Examiner	Art Unit	
	Stuart Hansen	2809	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-20 and 22-33* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 3/30/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Application (10/529,615) filed 3/30/2005. It is recognized that this invention is also in the PCT national phase (PCT/SG03/00091, filed 4/17/2003) and is eligible for Foreign Priority under SG200205929-3 (filed 9/30/2002).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 22-25 and 33 rejected under 35 U.S.C. 102(e) as being unpatentable by Koike (US 6,519,165 B2, filed 11/29/2001, dated 2/11/2003).

Koike teaches the device according to claim 22: A switch mode power supply (Fig 1) comprising: a transformer (Fig 1 [2]), a transistor (Fig 1 [3]) coupled to control the current through a primary (Fig 1 [14]) of the transformer (Fig 1 [2]), a control unit (Fig 1 [7]) configured to control switching of the transistor (Fig 1 [3]) to generate current pulses in the transformer (Fig 1 [2]), a memory device (Fig 1 [11]) for storing date indicating whether the switching mode power supply is operating in a first power supply mode, and

a current limitation circuit (Fig 1 [12]) arranged to receive a first signal (Fig 1 [30]) indicative of the current through the primary of the transformer and to limit the current pulses if the first signal indicates that the current is above a threshold value (Fig 1 [42]) and the memory device (Fig 1 [11]) indicates that the switching mode power supply is operating in the first power supply mode (column 7, lines 43-57).

Claim 23 is further taught by Koike: the control unit (Fig 1 [7]) is a single integrated circuit logic device (column 10, lines 14-18)

According to Koike, the device according to claim 24 is also taught: the threshold value is on a value received at a pin input of the logic device (column 10, lines 14-18).

Regarding claim 25, Koike further teaches: the threshold value has a value determined by an internal reference voltage (Fig 1 [42]) of the integrated circuit (column 10, lines 14-18).

Koike also teaches claim 33: A method of operating a power supply having a transformer (Fig 1 [2]), a transistor (Fig 1 [3]) controlling the current through a primary of the transformer, and a control unit (Fig 1 [7]) for controlling the switching of the transistor to generate current pulses in the transformer, the method comprising: a) receiving a signal (Fig 1 [30]) indicative of the current through the primary of the transformer, and b) limiting the current pulses if the signal indicates that the current is above a threshold value (Fig 1 [42]) and if the power supply is operating in a first power supply mode of a plurality of power supply modes (column 6, lines 33-49; column 7, lines 43-57).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14-16 and 26-29 are rejected under 35 U.S.C. 103(a) as obvious over Kitano (US 6,563,720 B2, filed 3/19/2002, dated 5/13/2003).

According to claim 14, Kitano teaches: A switching mode power supply (Fig 8 [1]) comprising: a transformer (Fig 8 [n]), a transistor (Fig 8 [q]) operably coupled to switch current through a primary (Fig 8 [n1]) of the transformer (Fig 8 [n]), and a control unit (Fig 8 [6]) configured to control the switching of the transistor (Fig 8 [q]) to generate current pulses through the transformer (Fig 8 [n]), the control unit (Fig 8 [6]) further configured to receive a signal from a secondary side of the transformer (Fig 8 [n]), the control unit (Fig 8 [6]) configured to enable switching of the transistor (Fig 8 [q]) in the case that a characteristic of the signal is outside the range in a first direction, and disabling switching of the transistor in the case that the characteristic of the signal is outside the range in a second direction (Column 2, lines 13-44).

Kitano lacks anticipation, however, by not teaching to: the control unit further configured to compare the signal (from the secondary side) with two threshold levels defining a range.

The invention as claimed would have been obvious to one of ordinary skill in the art at the time of the invention to send the signal from the secondary side of the transformer back to the primary side of the transformer for the sake of compacting all control components onto a single side of the transformer making it possible to cut down on the total number of parts necessary and even perhaps enabling all converter controls to be placed onto a single circuit board.

Regarding claim 15, Kitano teaches: the control unit (Fig 8 [6]) is further configured to enable switching when the characteristic of the signal is above a first threshold value, and disable switching of the transistor (Fig 8 [q]) in the case that the characteristic of the signal is below a second lower value (column 2, lines 24-44).

Kitano lacks anticipation, however, by not teaching: the characteristic of the signal is inversely related to power drawn by a load coupled to the secondary side.

It would have been obvious to one of ordinary skill in the art at the time of the invention to make: the characteristic of the signal is inversely related to power drawn by a load coupled to the secondary; simply by reversing the terminals of the comparators [12 & 13] for the purpose of easily controlling some input value of the controller in an opposite direction of the output voltage, i.e. output voltage decreases so duty cycle should increase.

According to claim 16, Kitano teaches: the characteristic of the signal is directly related to the power drawn by a load coupled to the secondary side, and wherein the control unit is further configured to enable switching when the characteristic of the signal is above a first threshold value, and disable switching of the transistor (Fig 8 [q]) in the

case that the characteristic of the signal is below a second lower threshold value (column 2, lines 24-44).

Regarding claim 26, Kitano teaches: A method of operating a power supply, the power supply having a transformer (Fig 8 [n]), a transistor (Fig 8 [q]) controlling the current through the primary of the transformer (Fig 8 [n]), and a control unit (Fig 8 [6]) for controlling the switching of the transistor (Fig 8 [q]) to generate current pulses in the transformer (Fig 8 [n]), the method including: a) receiving a signal (Fig 8 [pc2]) from the secondary side of the transformer (Fig 8 [n]), and b) enabling switching of the transistor (Fig 8 [q]) in the case that the characteristic of the signal is outside the range in a first direction and disabling switching to the transistor (Fig 8 [q]) in the case that the characteristic of the signal is outside the range in a second direction.

Kitano lacks anticipation though, by not: receiving a signal from a secondary side of the transformer and comparing a characteristic of the signal with two threshold levels, the two threshold levels defining a range therebetween.

It would have been obvious to one of ordinary skill in the art at the time of the invention that the device according to Kitano should send the signal to the controller before comparing it to two threshold values, because this allows all of the controlling components to exist on one side of the transformer, minimizing space consumption, possibly reducing the number of components necessary, and opening up the possibility of having all components on a single circuit board.

With reference to claim 27, Kitano teaches: wherein step b) further comprises enabling switching when the characteristic of the signal is above a first threshold value,

and disable switching of the transistor in the case that the characteristic of the signal is below a second lower value (column 2, lines 24-44).

Kitano lacks anticipation though by not teaching: the characteristic of the signal is inversely related to power drawn by a load coupled to the secondary side.

It would have been obvious to one of ordinary skill in the art at the time of the invention that the characteristic of the signal could easily be inversely related to power drawn by a load coupled to the secondary side of the transformer by switching the terminals of comparators [12 & 13] for the purpose of changing one variable in an opposite direction to that of the change in the output voltage.

According to claim 28, Kitano teaches: the characteristic of the signal is directly related to the power drawn by a load coupled to the secondary side, and wherein step b) further comprises enabling switching when the characteristic of the signal is above a first threshold value, and disable switching of the transistor in the case that the characteristic of the signal is below a second lower threshold value (column 2, lines 24-44).

Kitano further teaches the method according to claim 29: wherein the characteristic of the signal comprises a magnitude of the signal (column 2, lines 24-44).

Claims 17 and 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Kitano (US 6,563,720 B2, filed 3/19/2002, dated 5/13/2003) as applied to claim 14 above, and further in view of Saito et al. (US 5,297,014, filed 1/3/1992, dated 3/22/1994).

Regarding claim 17 Kitano lacks anticipation by not teaching: a blanking window definition circuit configured to prevent the control unit from disabling switching of the transistor in the case that the signal is below the second lower threshold value for less than a preset period of time.

Saito et al. however does teach: a blanking window definition circuit (Fig 4 [8]) configured to prevent the control unit from disabling switching of the transistor in the case that the signals is below the second lower threshold value for less than a preset period of time (column 4, lines 59-68; column 5, lines 1-7: the delay circuit [8] is in place to prevent any overload protection from causing interruptions due to load inrush currents).

This combination would have been obvious to one of ordinary skill in the art at the time of the invention because both inventions are switch mode power supplies with feedback signals from the secondary side of a transformer for the purpose of providing more reliable and yet safe power. It is also well known that many loads require a large inrush current when performing tasks such as starting motors, and that this inrush is temporary and the load current will settle out at some lower value, therefore a delay in the signal from the output signal to the input controller creates a window, in which loads are allowed to start and get into a smooth running mode before having power cut off.

Regarding claim 30 Kitano lacks anticipation by not teaching: preventing the control unit from disabling switching of the transistor in the case that the signal is below the second lower threshold value for less than a preset period of time.

Saito et al. however does teach: preventing (Fig 4 [8]) the control unit from disabling switching of the transistor in the case that the signal is below the second lower threshold value for less than a preset period of time (column 4, lines 59-68; column 5, lines 1-7: the delay circuit of Figure 4 [8] is in place to prevent any overload protection from causing interruptions due to load inrush currents).

This combination would have been obvious to one of ordinary skill in the art at the time of the invention because both inventions are switch mode power supplies with feedback signals from the secondary side of a transformer for the purpose of providing more reliable and yet safe power. It is also well known that many loads require a large inrush current when performing tasks such as starting motors, and that this inrush is temporary and the load current will settle out at some lower value, therefore a delay in the signal from the output signal to the input controller creates a window, in which loads are allowed to start and get into a smooth running mode before having power cut off.

Claims 18, 19, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitano (US 6,563,720 B2, filed 3/19/2002, dated 5/13/2003) as applied to claim 14 above, and further in view of Koike (US 6,519,165 B2, filed 11/29/2001, dated 2/11/2003).

In respect to claim 18, Kitano fails to disclose: a current limitation circuit arranged to receive a second signal indicative of the current through the primary of the transformer and to limit the current pulses if the second signal indicates that the current through the primary of the transformer is above a threshold value.

Koike, however, does teaches: a current limitation circuit (Fig 1 [12]) arranged to receive a second signal (Fig 1 [30]) indicative of the current through the primary (Fig 1 [14]) of the transformer (Fig 1 [2]) and to limit the current pulses if the second signal (Fig 1 [30]) indicates that the current through the primary (Fig 1 [14]) of the transformer (Fig 1 [2]) is above a threshold value (Fig 1 [42], column 6, lines 33-49).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the current limitation circuit of Koike to the DC-DC voltage converter of Kitano because they are both in the related area of DC-DC voltage conversion via transformers. This combination is beneficial for the purpose of power supply and converter protection from over-current damage to the switching device or the primary side winding.

Koike teaches the limitations of claim 19: a memory device (Fig 1 [11]) for storing data indicating whether the switching mode power supply is operating in a first power supply mode, and arranged to enable the current limitation circuit only in the case that the power supply is operating in first power supply mode (column 7, lines 43-57; The mode selector switch (Fig 3 [61]) can be viewed as either storing a '0' when the switch is closed to ground or a '1' when it is open and separate from ground, and if the system goes into a standby mode the other circuitry would be disabled, and only enabled once back into standard mode.).

With regard to claim 31, Kitano fails to disclose: c) receiving a second signal indicative of the current through the primary of the transformer and limiting the current pulses if the second signal indicates that the current is above a threshold value.

Koike teaches the method of claim 31: c) receiving a second signal indicative of the current through the primary of the transformer (Fig 1 [I_1])and limiting the current pulses if the second signal indicates that the current is above a threshold value (Fig 1 [42]; column 6, lines 33-49).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the current limitation capabilities of Koike to the DC-DC voltage conversion process of Kitano because they are both in the related area of DC-DC voltage conversion via transformers. This combination is beneficial for the purpose of power supply and converter protection from over-current damage to the switching device or the primary side winding.

Regarding claim 32, Koike further teaches: performing step c) only in the case that the power supply is operating in a first power supply mode of a plurality of power supply modes (column 7, lines 43-57; If the mode selector detects that the power supply is in standby mode, the overcurrent protection circuit is effectively disabled because no current flows through the primary transformer inductance).

Claims 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitano (US 6,563,720 B2, filed 3/19/2002, dated 5/13/2003) and Koike (US 6,519,165 B2, filed 11/29/2001, dated 2/11/2003) as applied to claim 19 above, and further in view of DiTommaso (US 6,271,707 B1, filed 5/14/1999, dated 8/7/2001).

With respect to claim 20, the combined circuit of Kitano and Koike lacks anticipation by not showing: the memory device comprises a flip flop.

DiTommaso however does teach a flip flop memory device (Fig 1 [20]) used for storing and output either a high or low value depending upon the inputs.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the flip flop of DiTommaso to substitute the memory device of Koike because this is a very well known and cost effective way of keeping track of the state (high/low, 1/0) of a single element for the purposes of reliability and simplistic circuit design.

Allowable Subject Matter

4. Claim 21 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not show a current limitation circuit that is a logic gate coupled to receive a logic signal from a flip flop.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stuart Hansen whose telephone number is 571-270-1611. The examiner can normally be reached on 7:30- 5 M-Th, Alt. Frid 7:30-4 Est Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-270-2100. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stuart Hansen

February 12, 2007

STEVEN LOKE
SUPERVISORY PATENT EXAMINER